**EEE-1212: Digital Logic Design Lab**

1st Year 2nd Semester

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**Experiment Number:** 07

**Name of the Experiment:**

a)Verification of a JK flip-flop

b) Design and construction of MOD-16 ripple counter.

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**Experiment name:**

7(a). Verification of a JK flip-flop

7(b). Design and construction of MOD-16 ripple counter.

**Objectives:**

1. Testing the IC-7476 and verify JK flip-flop.
2. Setting up the circuit of a MOD-16 ripple counter.

**Theory:**

**Flip-flop:**

The most important memory element is the flip-flop, which is made up of an assembly of logic gates. Even though a logic gate, by itself, has no storage capability, several can be connected together in ways that permit information to be stored. Several different gate arrangements are used to produce these flip-flops (abbreviated FF).

**JK Flip-flop:**

The J-K flip-flop is the most versatile of the basic [flip-flops](http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/flipflop.html#c1). It has the input- following character of the clocked [D flip-flop](http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/dflipflop.html#c3) but has two inputs, traditionally labeled J and K. If J and K are different then the output Q takes the value of J at the next clock edge. The J and K inputs control the state of the FF in the same ways as the S and R inputs do for the clocked S-R flip-flop except for one major difference: the J=K=1 condition does not result in an ambiguous output. For this 1, 1 condition, the FF will always go to its opposite state upon the negative transition of the clock signal. This is called the toggle mode of operation. If J and K are both low then no change occurs.

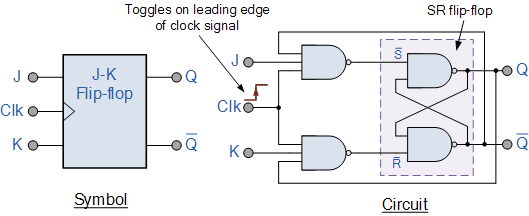


Fig: JK Flip-flop

**Ripple Counter:**

A ripple counter is an asynchronous counter where only the first flip-flop is clocked by an external clock. All subsequent flip-flops are clocked by the output of the preceding flip-flop. Asynchronous counters are also called ripple-counters because of the way the clock pulse ripples it way through the flip-flops.

The MOD of the ripple counter or asynchronous counter is 2n if n flip-flops are used. For a 4-bit counter, the range of the count is 0000 to 1111 (24-1).

The following points concerning its operation:

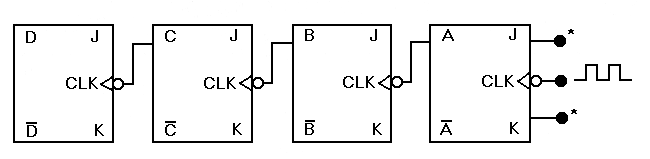


Fig: Four-bit asynchronous (ripple) counter

1. The clock pulses are applied only to the CLK input of flip-flop A. Thus, flip-flop A will toggle (change to its opposite state) each time the clock pulses make a negative (HIGH-to-LOW) transition. Note that J K 1 for all FFs.

2. The normal output of flip-flop A acts as the CLK input for flip-flop B, and so flip-flop B will toggle each time the A output goes from 1 to 0. Similarly, flip-flop C will toggle when B goes from 1 to 0, and flip-flop D will toggle when C goes from 1 to 0.

3. FF outputs D, C, B, and A represent a four-bit binary number, with D as the MSB. Let’s assume that all FFs have been cleared to the 0 state (CLEAR inputs are not shown). The waveforms in Figure 7-1 show that a binary counting sequence from 0000 to 1111 is followed as clock pulses are continuously applied.

4. After the NGT of the fifteenth clock pulse has occurred, the counter FFs are in the 1111 condition. On the sixteenth NGT, flip-flop A goes from 1 to 0, which causes flip-flop B to go from 1 to 0, and so on, until the counter is in the 0000 state. In other words, the counter has gone through one complete cycle (0000 through 1111) and has recycled back to 0000. From this point, it will begin a new counting cycle as subsequent clock pulses are applied.

**Instruments:**

1. A Trainer Board
2. IC(s) IC-7476
3. Connecting wires
4. Clock pulse

**Procedure (a):**

1. At first we placed the integrated circuit with IC-7476 on a breadboard properly. This IC is placed across the gap in the center of the breadboard.
2. Then we connected the inputs of the logic gate to the logic sources and its output to the logic indicator.
3. We gave biasing to the ICs with the VCC (5 volt) and GND (0 volt).
4. Then we implemented the logic circuits using logic gates and obtained equations. We connected the inputs with input switches and the output with output LEDs. The output of the circuit will be shown on the LED. (LED Off = 0, LED On = 1).
5. We observed outputs for various input combination.

**Procedure (b):**

1. At first we placed the integrated circuit with IC-7476(each IC contains two JK flip-flops) on a breadboard properly. This IC is placed across the gap in the center of the breadboard.
2. We gave biasing to the ICs with the VCC (5 volt) and GND (0 volt).
3. We applied the clock pulses only to the CLK input of flip-flop A and the CLK input of flip-flop B, C, D is respectively the output of A, B, C flip-flop.
4. The output of each flip-flop is connected to the LED light from which we can get our expected outputs.
5. We observed outputs for different frequency of clock pulses.

**Result (a):**

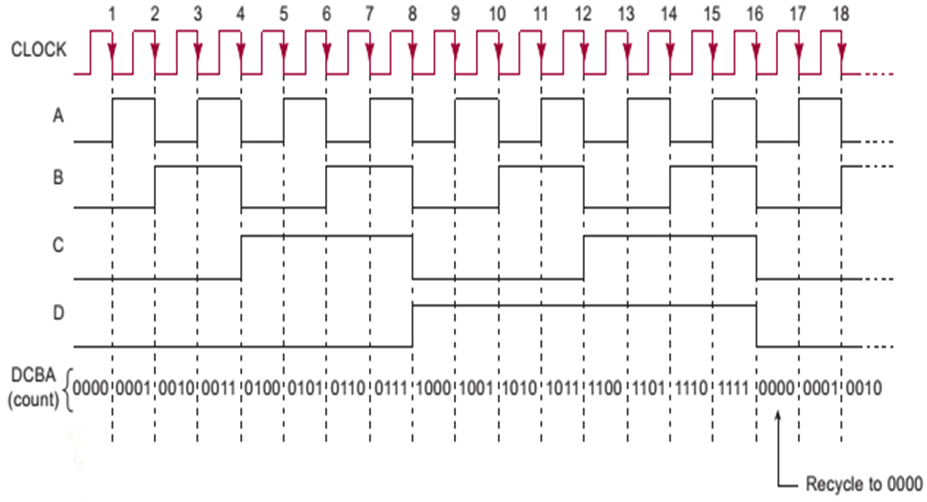
Truth table of JK flip-flop:

|  |  |  |  |
| --- | --- | --- | --- |
| J | K | CLK | Q |
| 0 | 0 | ↓ | No change |
| 0 | 1 | ↓ | 1 |
| 1 | 0 | ↓ | 0 |
| 1 | 1 | ↓ | Toggle |

**Result (b):**

We saw the output by the following sequences:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Serial no | D | C | B | A |
| 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 0 | 1 |
| 3 | 0 | 0 | 1 | 0 |
| 4 | 0 | 0 | 1 | 1 |
| 5 | 0 | 1 | 0 | 0 |
| 6 | 0 | 1 | 0 | 1 |
| 7 | 0 | 1 | 1 | 0 |
| 8 | 0 | 1 | 1 | 1 |
| 9 | 1 | 0 | 0 | 0 |
| 10 | 1 | 0 | 0 | 1 |
| 11 | 1 | 0 | 1 | 0 |
| 12 | 1 | 0 | 1 | 1 |
| 13 | 1 | 1 | 0 | 0 |
| 14 | 1 | 1 | 0 | 1 |
| 15 | 1 | 1 | 1 | 0 |
| 16 | 1 | 1 | 1 | 1 |



**Discussion:**

In this experiment we had to construct a MOD-16 ripple counter. We also have to test the IC-7476. We constructed the circuit in the bread board using the IC’s but faced lots of problem during the experiment and our experiment failed to show expected outputs but when we experimented it next day it showed expected results.

1. At first we tested the IC-7476 and it has two JK flip-flops. We worked with both FFs and found the desired result.
2. Then we started to construct a MOD-16 ripple counter using two IC-7476 as we need four flip-flops.
3. After completing the circuit we found that one of our ICs was not working and we changed that IC.
4. Again it was showing wrong outputs and we could not find that what we did wrong. Then we were asked to construct MOD-8 ripple counter.
5. We constructed the MOD-8 ripple counter and again we got wrong outputs. We were unable to find our mistakes.
6. And then we constructed MOD-4 ripple counter. It was also not showing the desired outputs.
7. But next day when we worked we took the clock pulse from the trainer board and our experiment succeeded.
8. Besides, we also faced some technical difficulties when using trainer board. But we figured them out but could not complete the experiment successfully first day. But we completed it successfully second day